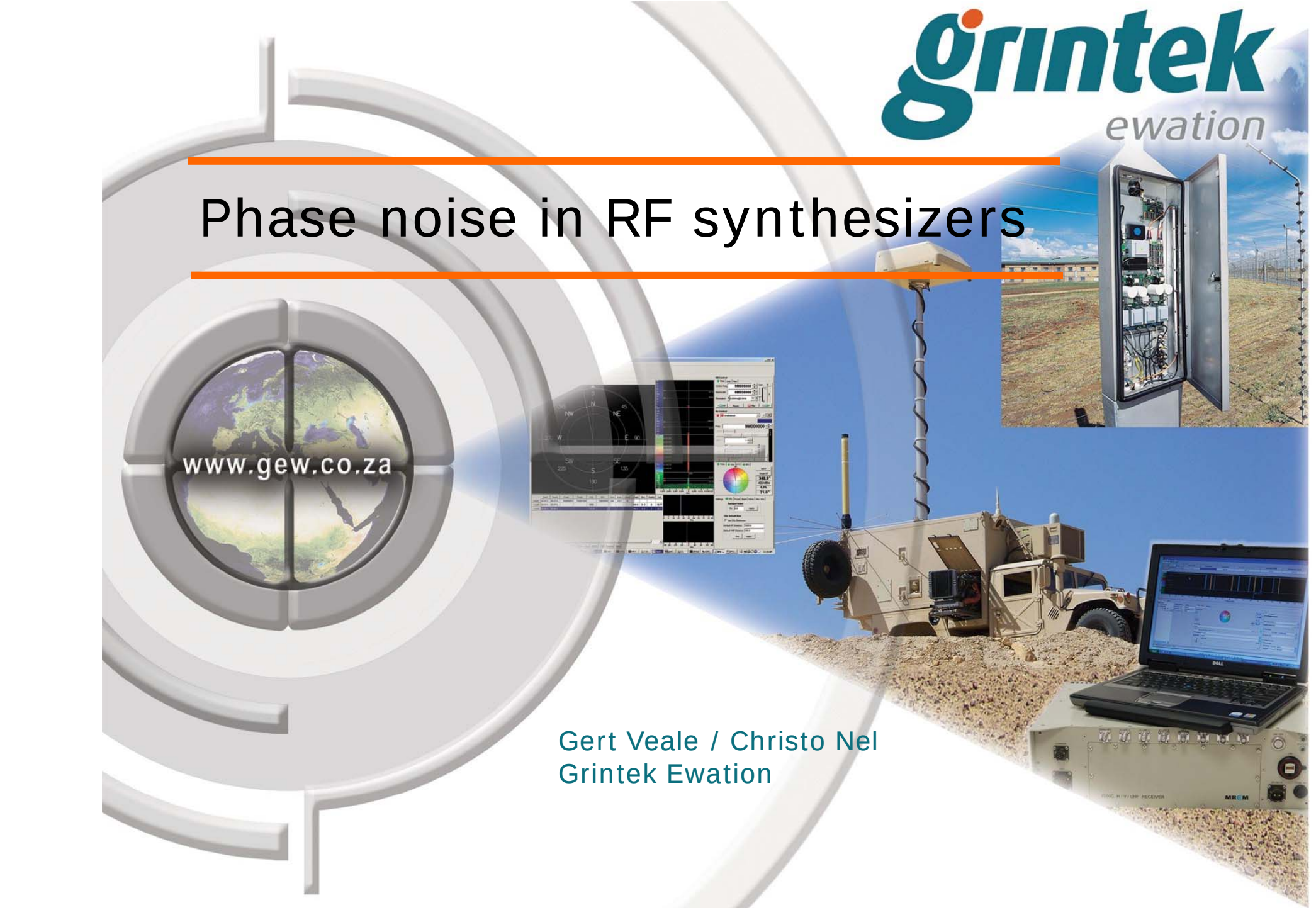
Phase noise in RF synthesizers

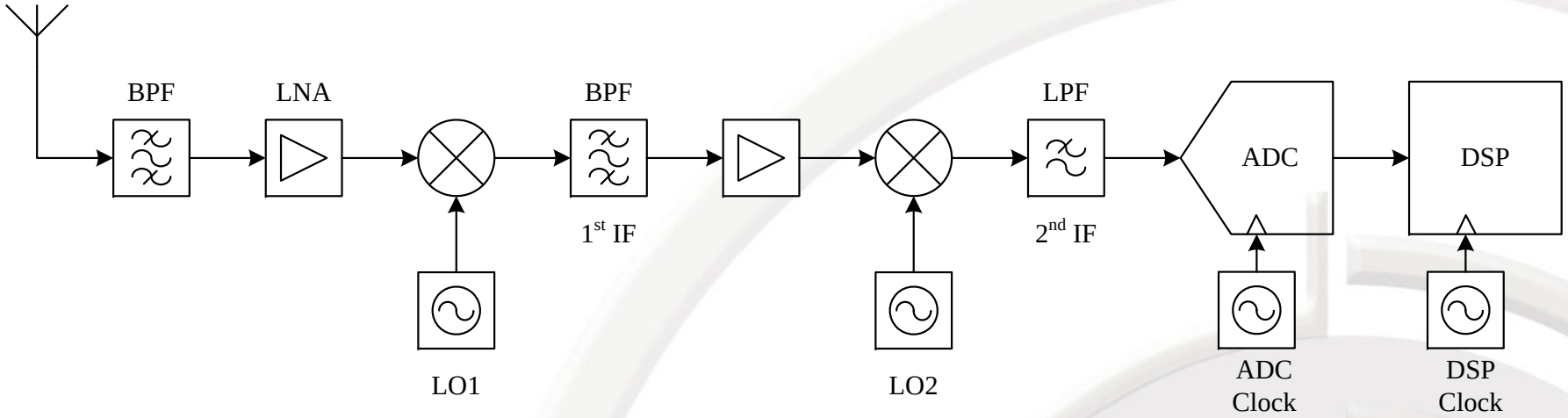


Gert Veale / Christo Nel
Grintek Ewation

Introduction & Overview

- Where are RF synthesizers used ?
- What is phase noise ?
- Phase noise effects
- Classic RF synthesizer architecture
- VCO phase noise modification
- In-band phase noise floor
- Optimum PLL loop bandwidth
- Conclusions

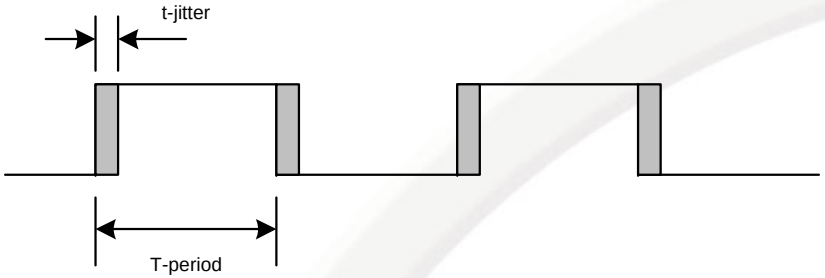
Where are RF synthesizers used?



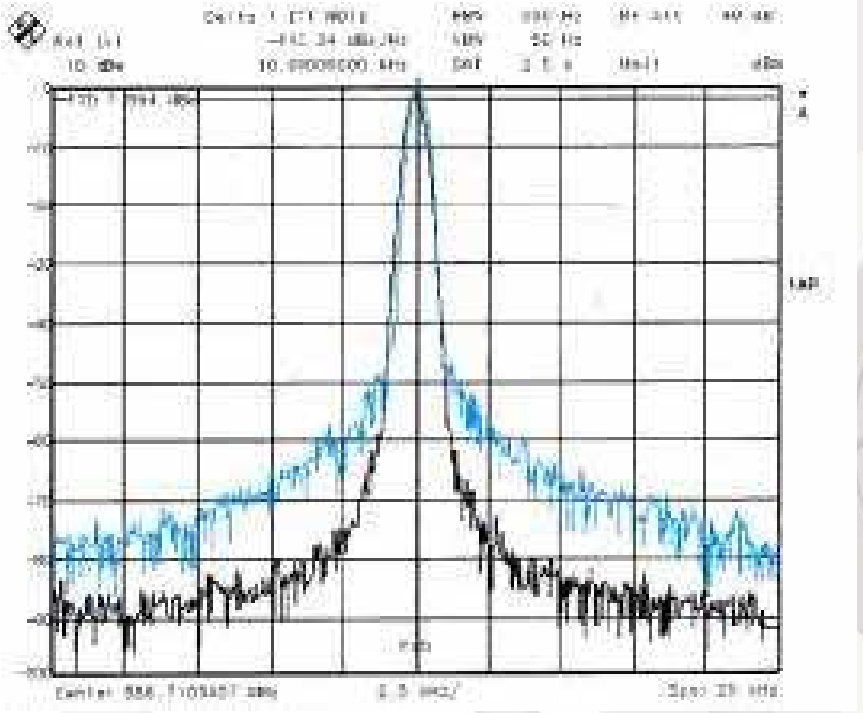
- Local oscillators (LOs) in receiver or transmitter architectures
- Digital clocks for analogue to digital converters (ADCs), digital to analogue converters (DACs) and other digital circuitry.

What is phase noise ?

- In the time domain it can be seen as jitter on a signal:

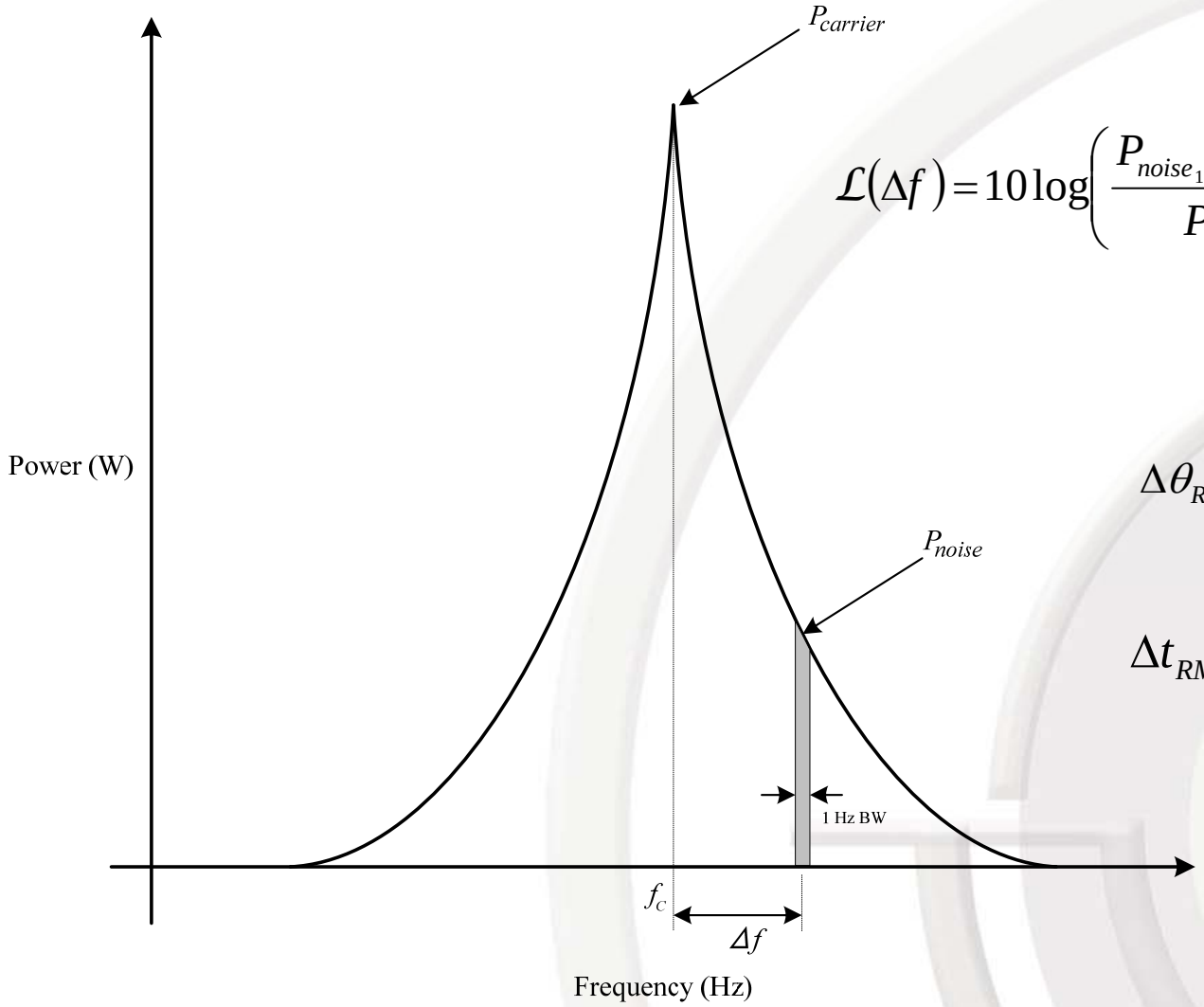


- In the frequency domain it presents itself as noise sidebands:



What is phase noise ?

- Mathematical Definition:



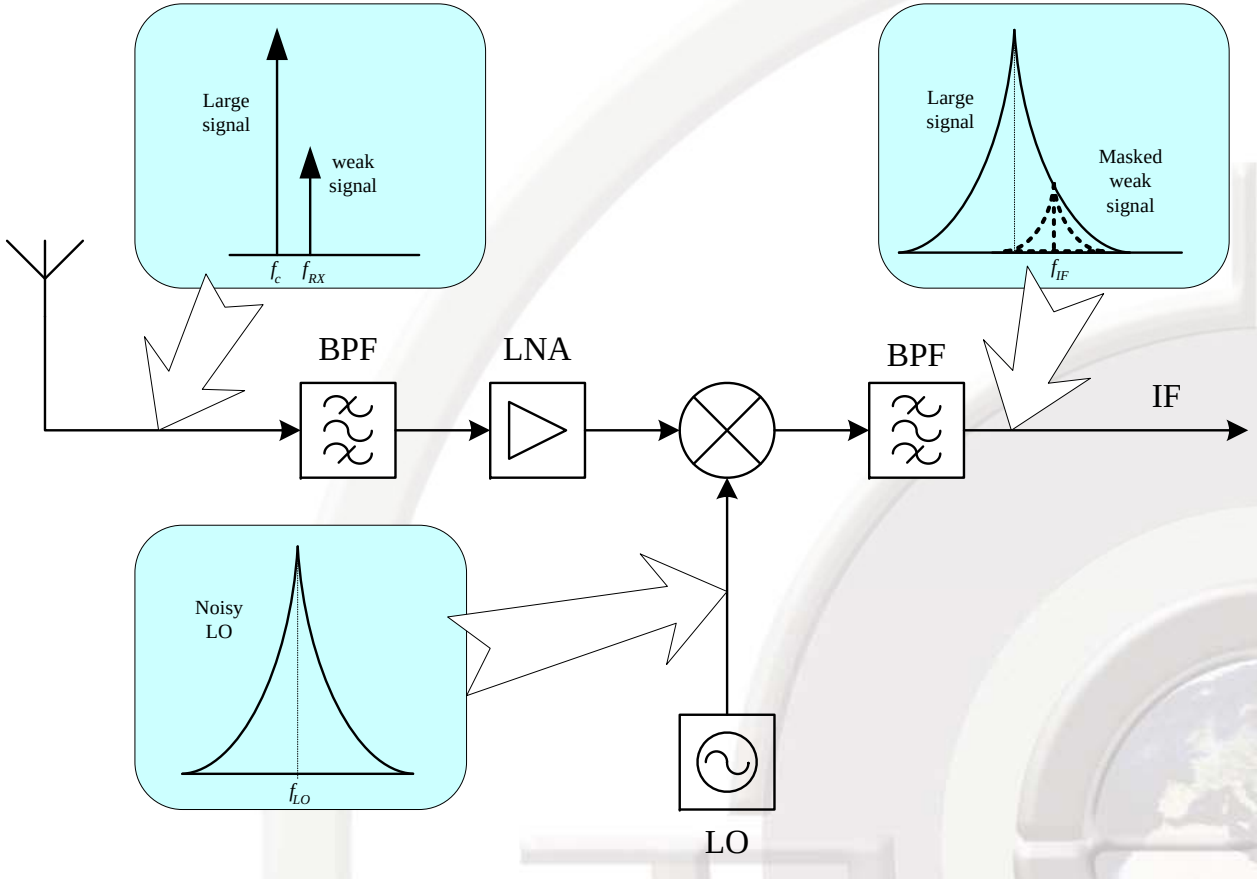
$$\mathcal{L}(\Delta f) = 10\log\left(\frac{P_{noise_{1\,Hz}} @ \Delta f}{P_{carrier}}\right) \quad \text{(dBc/Hz)}$$

$$\Delta\theta_{RMS} = \sqrt{2\int_{f_1}^{f_2} 10^{\frac{\mathcal{L}(f)}{10}}\, df} \quad \text{(rad)}$$

$$\Delta t_{RMS} = \frac{\Delta\theta_{RMS}}{2\pi\, f_o} \quad \text{(s)}$$

Phase noise effects

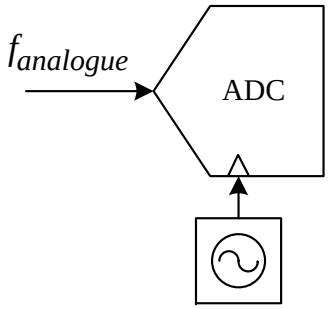
- Receiver reciprocal mixing with a noisy LO:



- Effect: Reduced receiver sensitivity in the presence of strong signals

Phase noise effects

- ADC clock with jitter:



ADC Clock with jitter

$$SNR_{FS} = -20\log\left(2\pi\ f_{analogue}\ \Delta t_{RMS}\right) \qquad \text{(dB)}$$

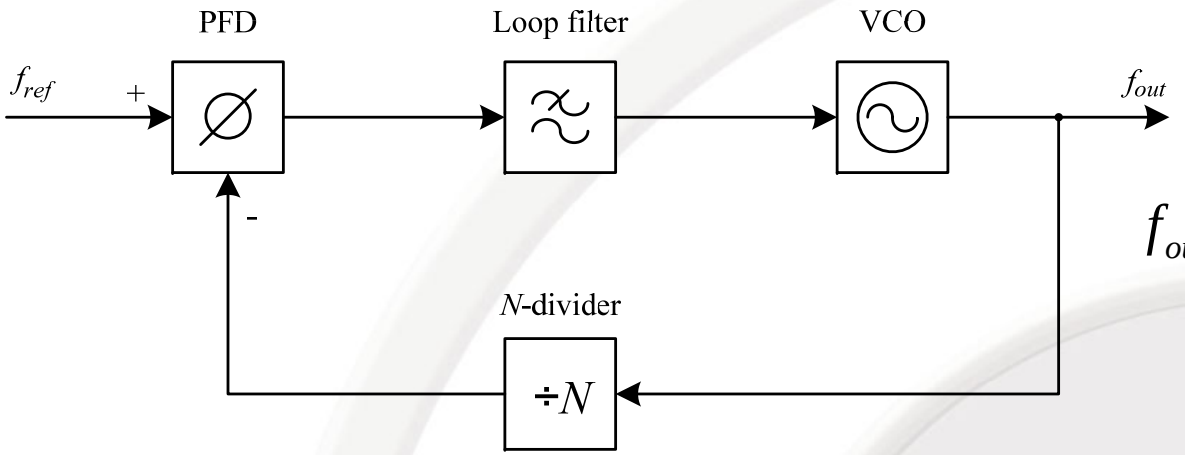
  - Result: Reduced full scale dynamic range

- Digital communication systems:

  - Result: Increased bit error rates (BERs) in phase modulated systems (QPSK, QAM etc.)

RF synthesizer architecture

- Consist of a classic phase locked loop (PLL) architecture:

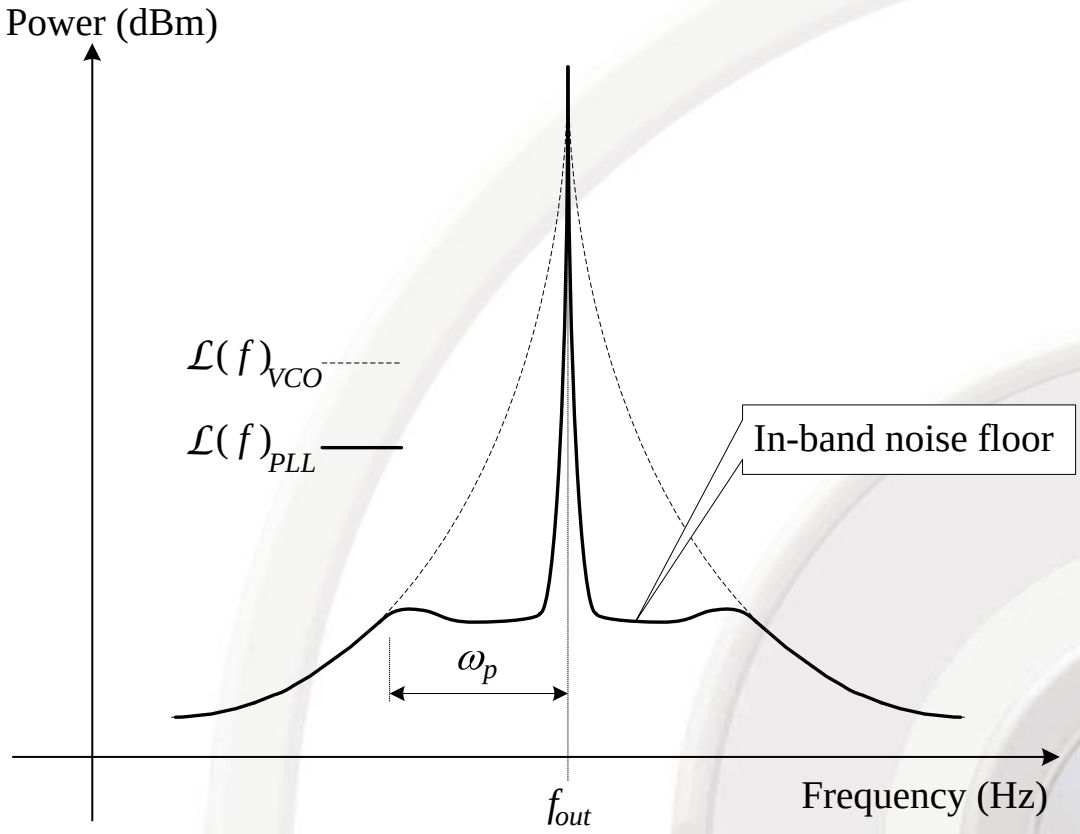


$$f_{out} = f_{ref} \cdot N$$

- Phase frequency detector (PFD)
- Loop filter
- Voltage controlled oscillator (VCO)
- Divider (N)

VCO phase noise in a PLL

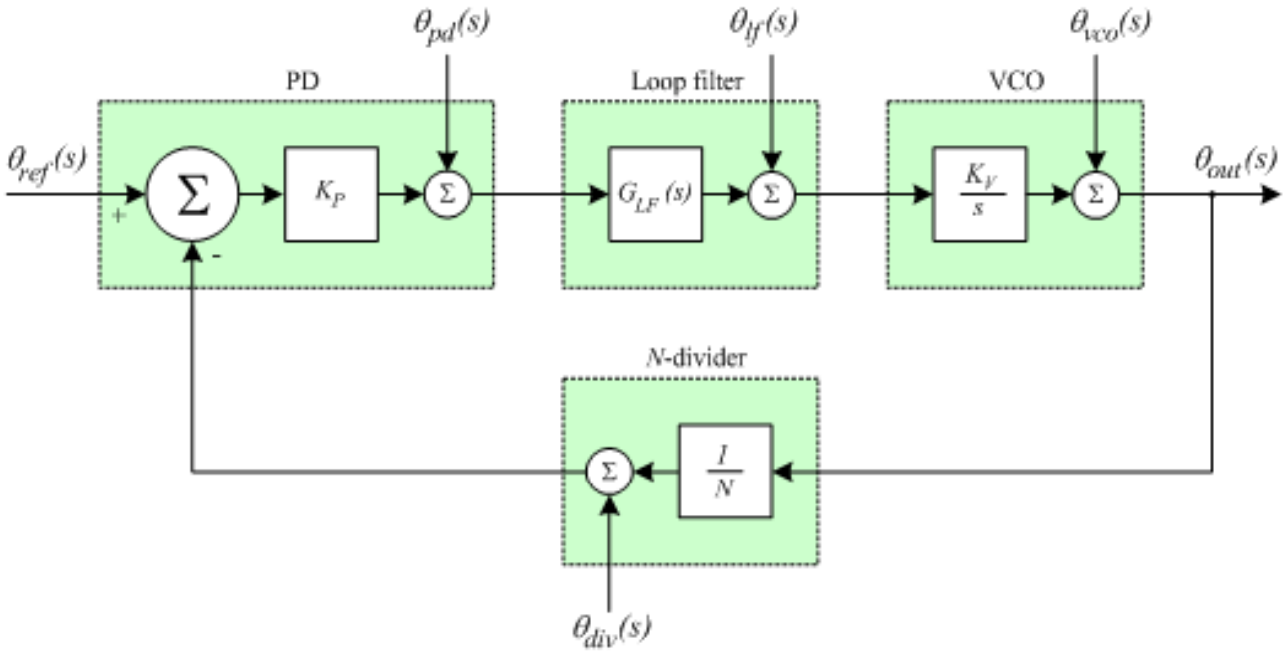
- VCO free running phase noise profile is altered by a PLL:



- An in-band noise floor $\mathcal{L}_{\text{in-band}}$ is formed within the PLL loop bandwidth ω_p
- You can “clean up” a noisy VCO with a well designed PLL

In-band PLL phase noise floor

- Consider the PLL linear model where each component has an associated noise source:



- Common Conclusion: $\mathcal{L}_{in\text{-}band}(\Delta f) \propto 20\log(N)$

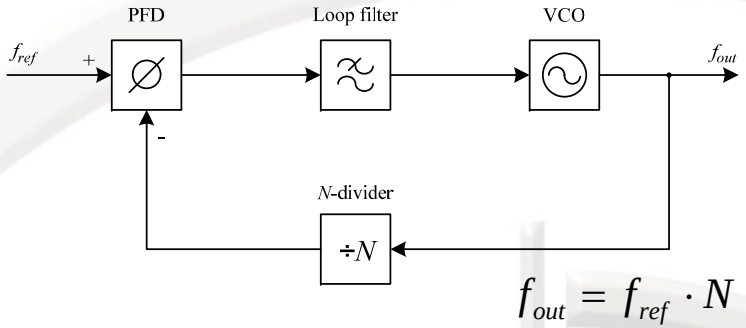
In-band PLL phase noise floor

- More exact:

$$\mathcal{L}_{in\text{-}band}(\Delta f) \propto 20\log N$$

$$\mathcal{L}_{in\text{-}band}(\Delta f) = 20\log N + \mathcal{L}_{PFD}(\Delta f)$$

$$= 20\log N + 10\log f_{ref} + FOM$$



- Interesting: $\mathcal{L}_{PFD}(\Delta f)$ increases with PFD operating frequency f_{ref}
- Figure of merit (FOM) or normalized noise floor ($\mathcal{L}_{1Hz}$) is device specific
- FOM is mainly determined by the random noise or time jitter inside the PFD:

$$FOM = \mathcal{L}_{1Hz} = 20\log(2\pi\Delta t_{PFD})$$

- The specific IC semiconductor process (CMOS, SiGe, GaAs etc.) has a huge impact on the FOM

In-band PLL phase noise floor

- Commercial RF synthesizer IC FOM comparison:

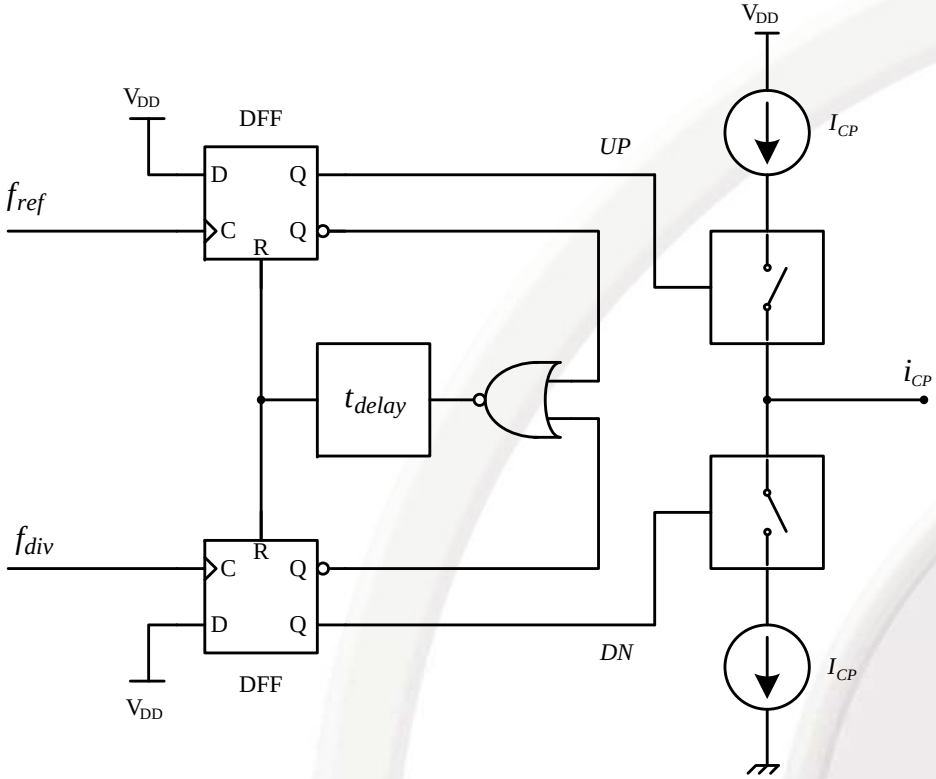
Device	Max Freq.	*N*-Divider	IC Process	FOM $\mathcal{L}_{1Hz}$	Power	Manufacturer
ADF4108	8 GHz	992 - 262175	0.35 µm BiCMOS	-119 dBc/Hz	0.08 W	Analog Devices
HMC700	8 GHz	32 - 65567	0.35 µm SiGe HBT	-226 dBc/Hz	0.36 W	Hittite Microwave
HMC440	2.8 GHz	2 - 32	GaAs HBT	-233 dBc/Hz	1.25 W	Hittite Microwave
HMC698	7 GHz	12 - 259	GaAs HBT	-233 dBc/Hz	1.55 W	Hittite Microwave

- Heterojunction bipolar transistor (HBT) designs tend to have better FOMs (Why ?)

- Devices with low *N*-Divider values and good FOMs normally dissipate a lot of power (Why ?)

In-band PLL phase noise floor

- FOM dependant on PFD noise, In a typical tri-state CP PFD we have:



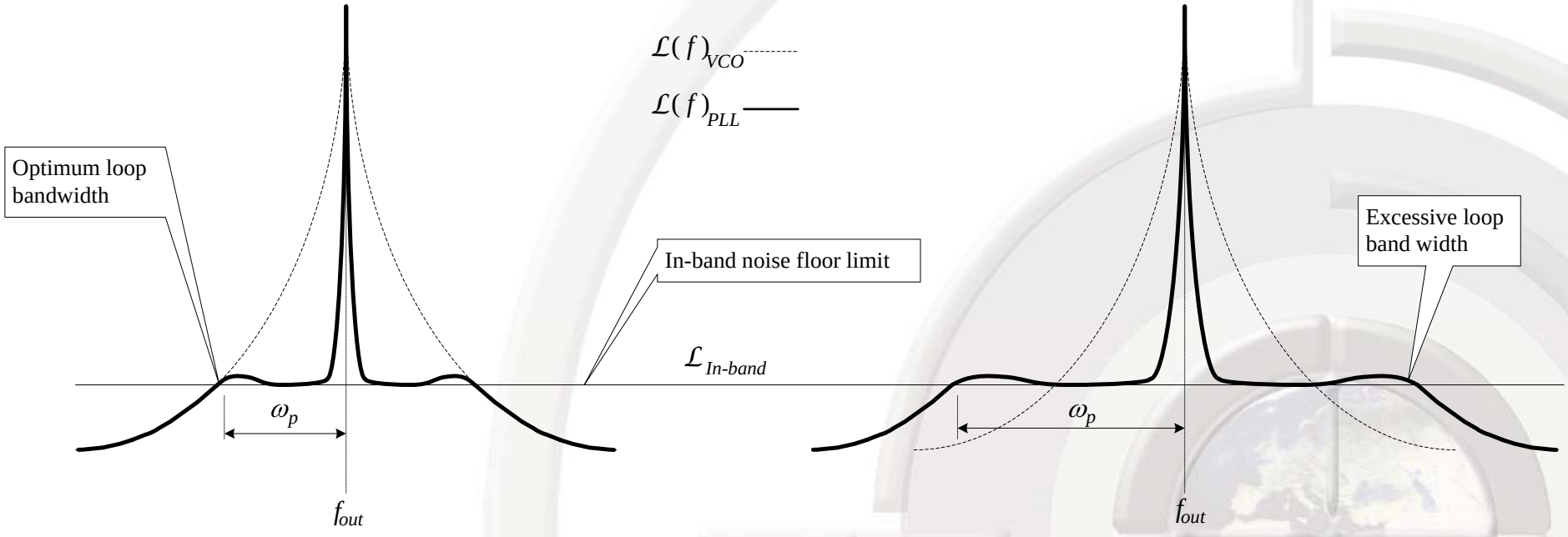
- t_{delay} is inserted to avoid the dead zone in the PFD
- Dead zone occurs when the current switches are not fast enough

- Charge pump noise current: $\overline{i_{CP}^2} \propto \frac{t_{delay}}{T_{ref}} \cdot I_{CP} \Delta f \quad \left(\mathrm{A}^2\right)$
- If designing a PFD, reduce t_{delay} for less PFD jitter and hence a better FOM:

$$FOM = 20\log\left(2\pi\Delta t_{PFD}\right)$$

Optimum PLL loop bandwidth

- Calculate $\mathcal{L}_{\text{in-band}}$ from device FOM and average *N*-divider etc.
- Compare with VCO datasheet and set PLL loop bandwidth ω_p to the VCO phase noise offset frequency that intersects with $\mathcal{L}_{\text{in-band}}$



- An incorrect loop bandwidth will cost you unnecessary phase noise
- Too small a loop bandwidth will also increase the PLL lock time

Conclusions

- Phase noise in synthesizers and its effects were shown
- The concept of PLL in-band phase noise was demonstrated
- To minimize PLL in-band phase noise, the following can be done:
  - Use low *N*-divider values
  - Use a high reference or PFD frequency f_{ref} (This will reduce the *N*-divider)
  - Use a device with a good FOM
- Optimize the PLL loop bandwidth for a given VCO phase noise profile