Digital Receiver

Experiment or Reality

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Contents

- Definition of a Digital Receiver.
- Advantages of using digital receiver techniques.
- Digital receivers: are they mysterious devices? Channelized receiver example.
- Practical implementation challenges.
- Pushing up the bandwidth.

Definitions

- Early microwave receivers consisted of RF component networks and devices which provided analog outputs which were displayed on CRT's.
  - Radar PPI
  - IFM polar display

- Later receivers, then called *digital receivers*, featured IFM's which provided digital output, and crystal video which was digitized into PW and amplitude information.

- Today we refer to ***digital receivers*** as receivers where the signal is sampled, quantized and processed without the aid of devices such as IFM's, phase discriminators or detectors.
  - In most cases, the input signal is amplified and converted to a suitable baseband before quantizing by superhet or similar RF networks.
  - Signal detection, and parameter measurements are then performed digitally by "software" based on mathematical algorithms.

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Getting rid of spurious and mismatch

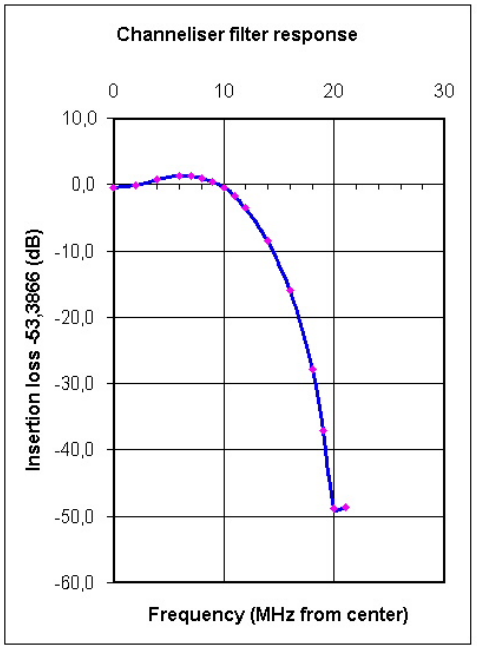
- When the signal is available in the digital domain, lossless and near perfect processing can be performed.
  - Example, MIXER

    - Input = $\cos(\omega_1 t)$
    - LO = $\cos(\omega_2 t)$
    - Output = $\cos(\omega_1 t) * \cos(\omega_2 t) = \cos(\pm\omega_1 \pm \omega_2)t$
  - What about: $A_1\cos(\pm 2\omega_1 \pm \omega_2)t$, $A_2\cos(\pm\omega_1 \pm 2\omega_2)t$, $A_2\cos(\pm 2\omega_1 \pm 2\omega_2)t$, $A_3\cos(\pm 3\omega_1 \pm \omega_2)t$, $A_n\cos(\pm n\omega_1 \pm m\omega_2)t$????

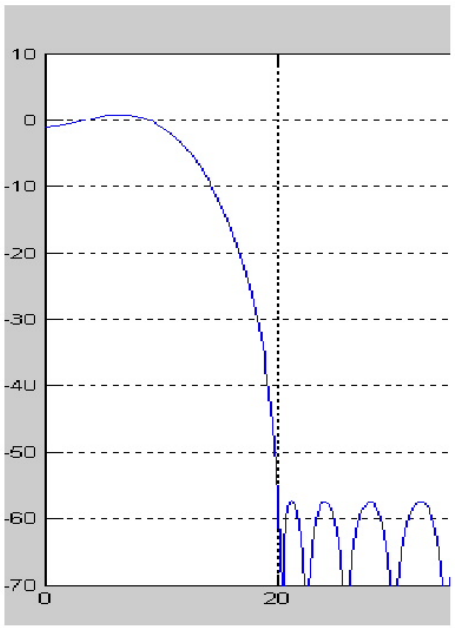
Getting the performance you design

- Mixing in the digital domain gives only the answer that you want.
- Filters perform as designed.

Measured



Designed



System advantages

- Once the signal is in the digital domain, more algorithms are possible than those provided by microwave devices.
  - Eg. Frequency measurement by rate of phase change instead of IFM gives much more accurate results.
- The same target hardware can be used for a variety of applications.
  - Eg. phase comparison and amplitude comparison DF systems can be implemented using by the same receiver hardware by changing the antenna arrangement and loading different software.

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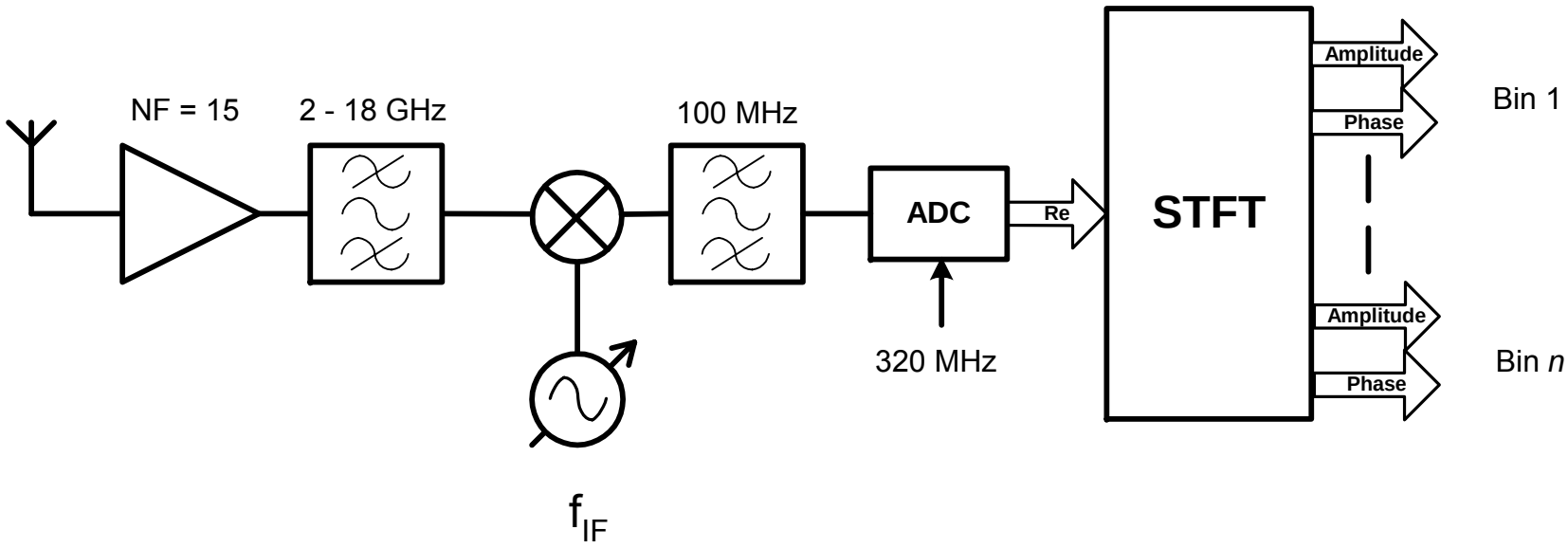
System level applications

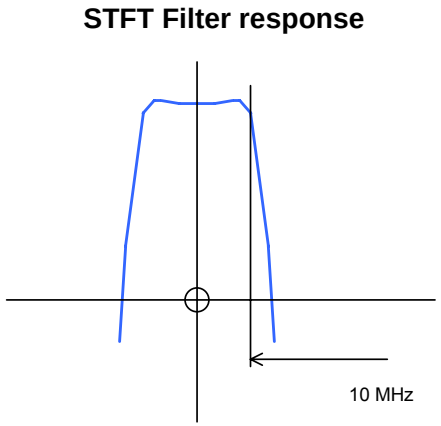
- Digital receivers can do the tasks that we are used to seeing in older receiver types, but do it better. From a system perspective there is nothing mysterious about digital receivers.
- Let's consider a Channelized receiver solution.
  - Older channelized receivers typically consisted of a superhet receiver, followed by a filterbank, and detectors at each filter output.
  - This allowed the detection of simultaneous signals in different filters (not without problems casued by filter response parasitics etc.).

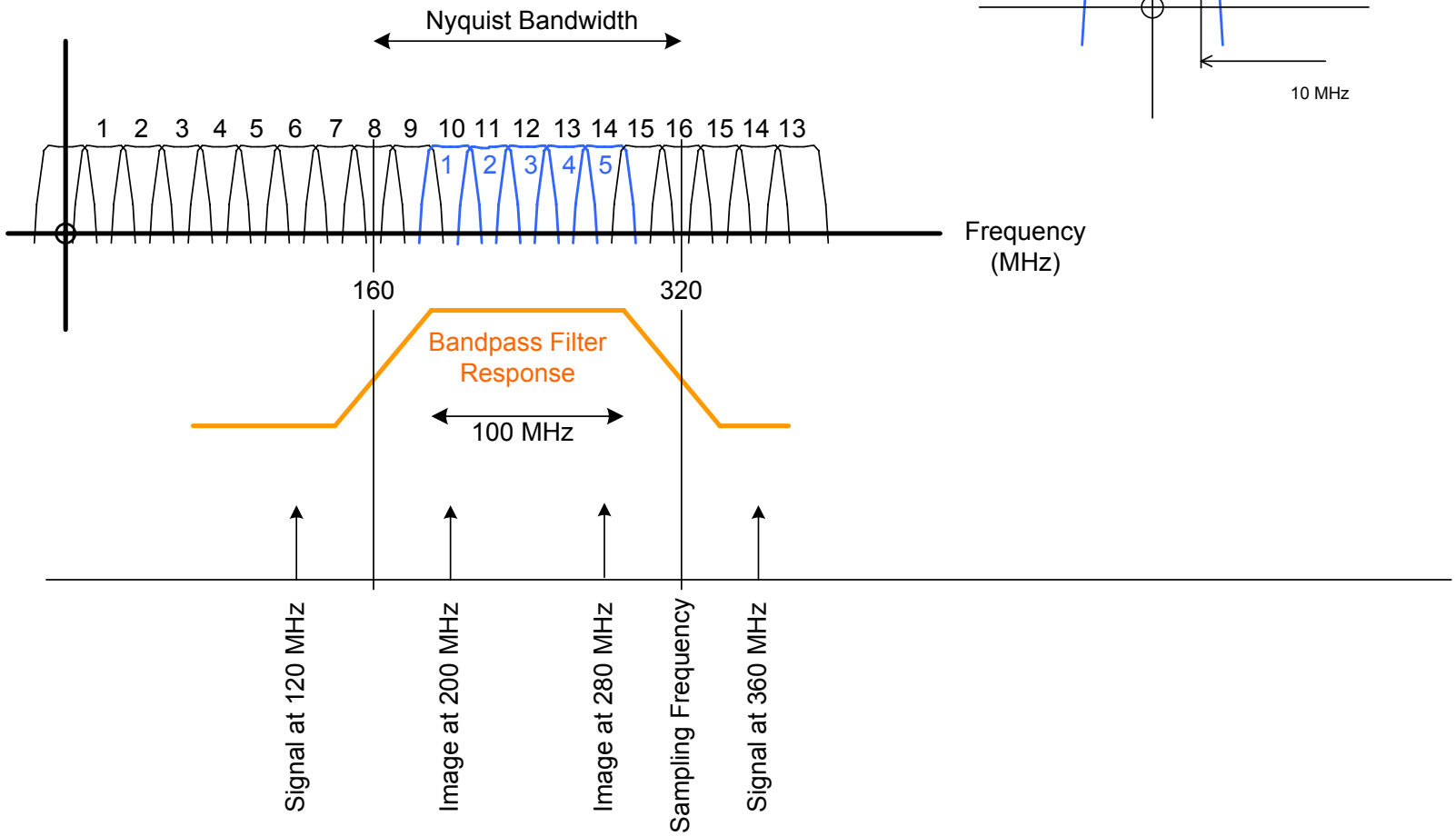
Digital receiver using digital filterbank



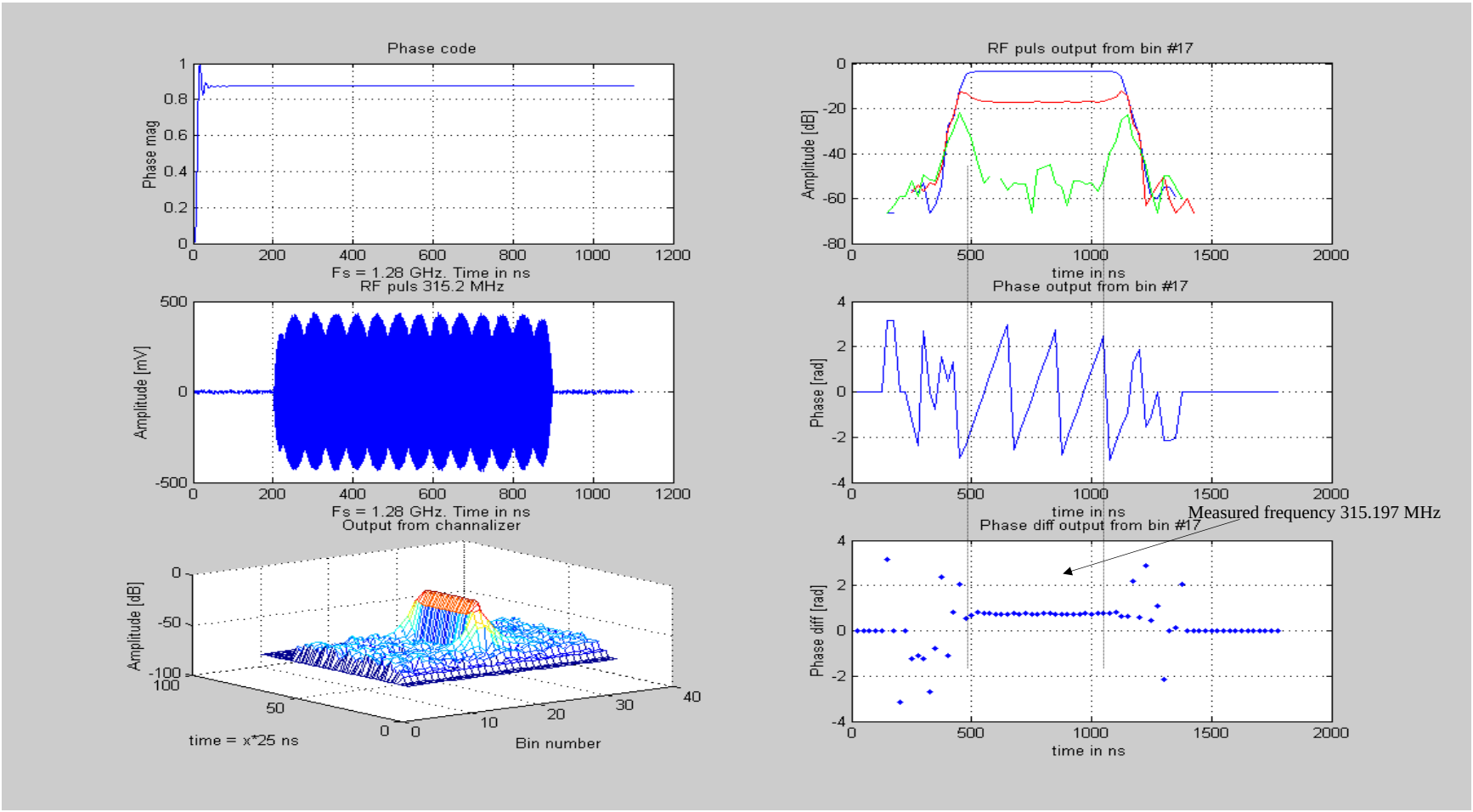
Digital filter implementation

Example: Using 16 point FFT frequency channelisation





Typical response with 8 to 10 bit quantizing

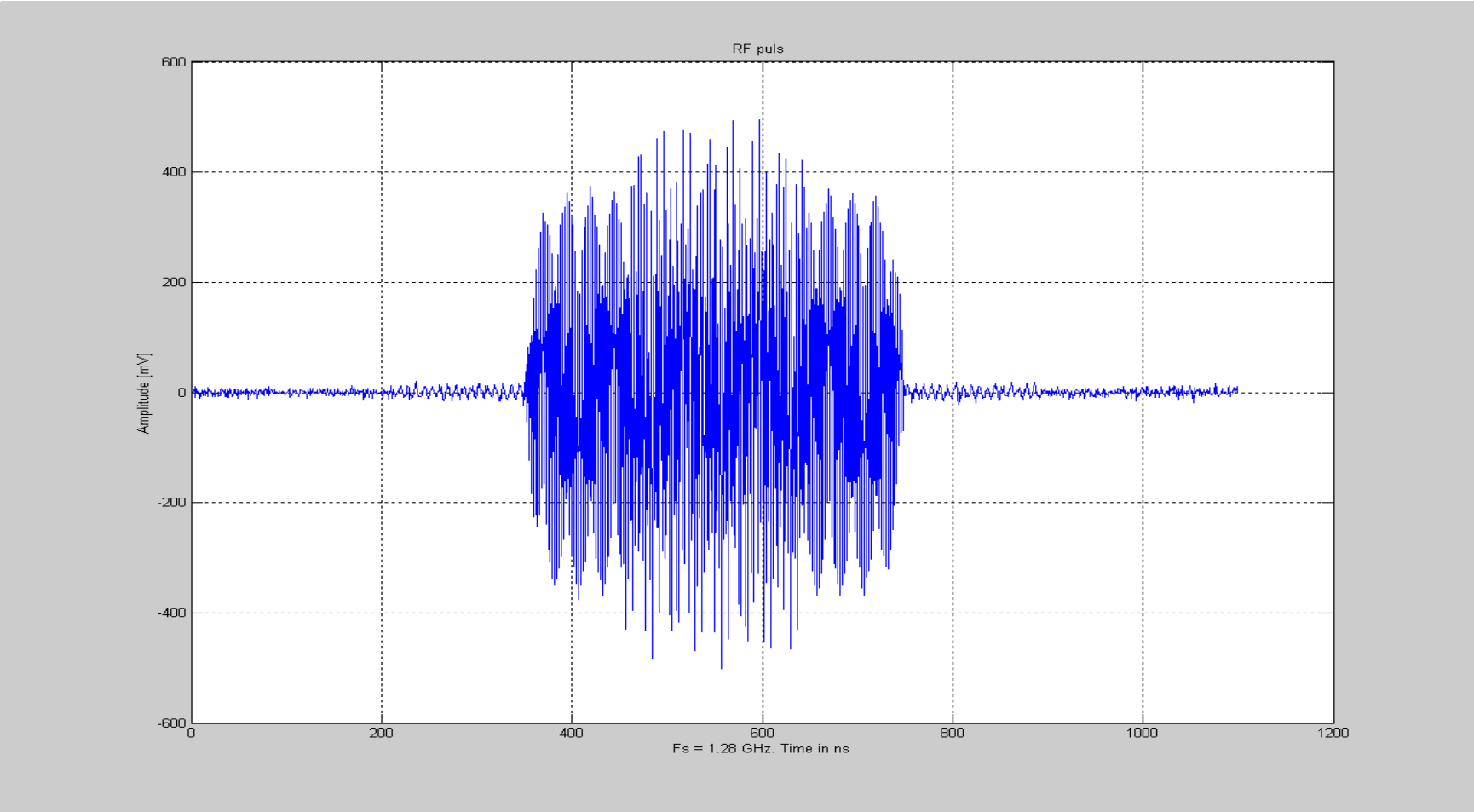


Simultaneous signal handling

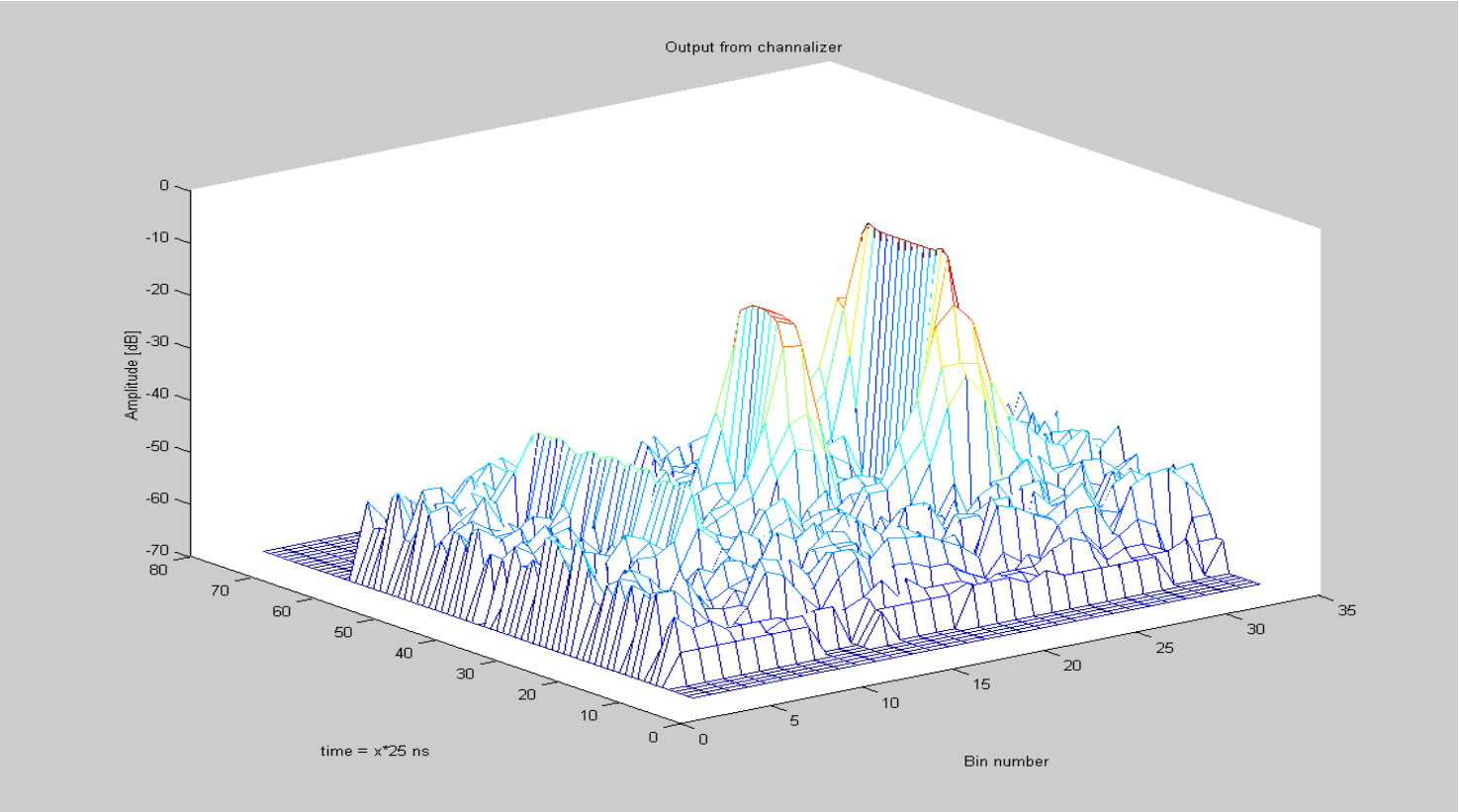
Digital receivers using multi-bit (8 or 10 bit) quantization allows the realization of a channelized receiver with sufficient dynamic range to allow the simultaneous measurement of signals in different frequency channels.

Parameter	Pulse 1	Pulse 2	Pulse 3
Baseband Frequency (MHz)	120.000	286.100	440.000
Pulse width (ns)	700	200	400
Amplitude (mV)	5.6	80	200
Input power ADC (dBm)	-35	-12	-4
System input (dBm)	-70	-47	-39

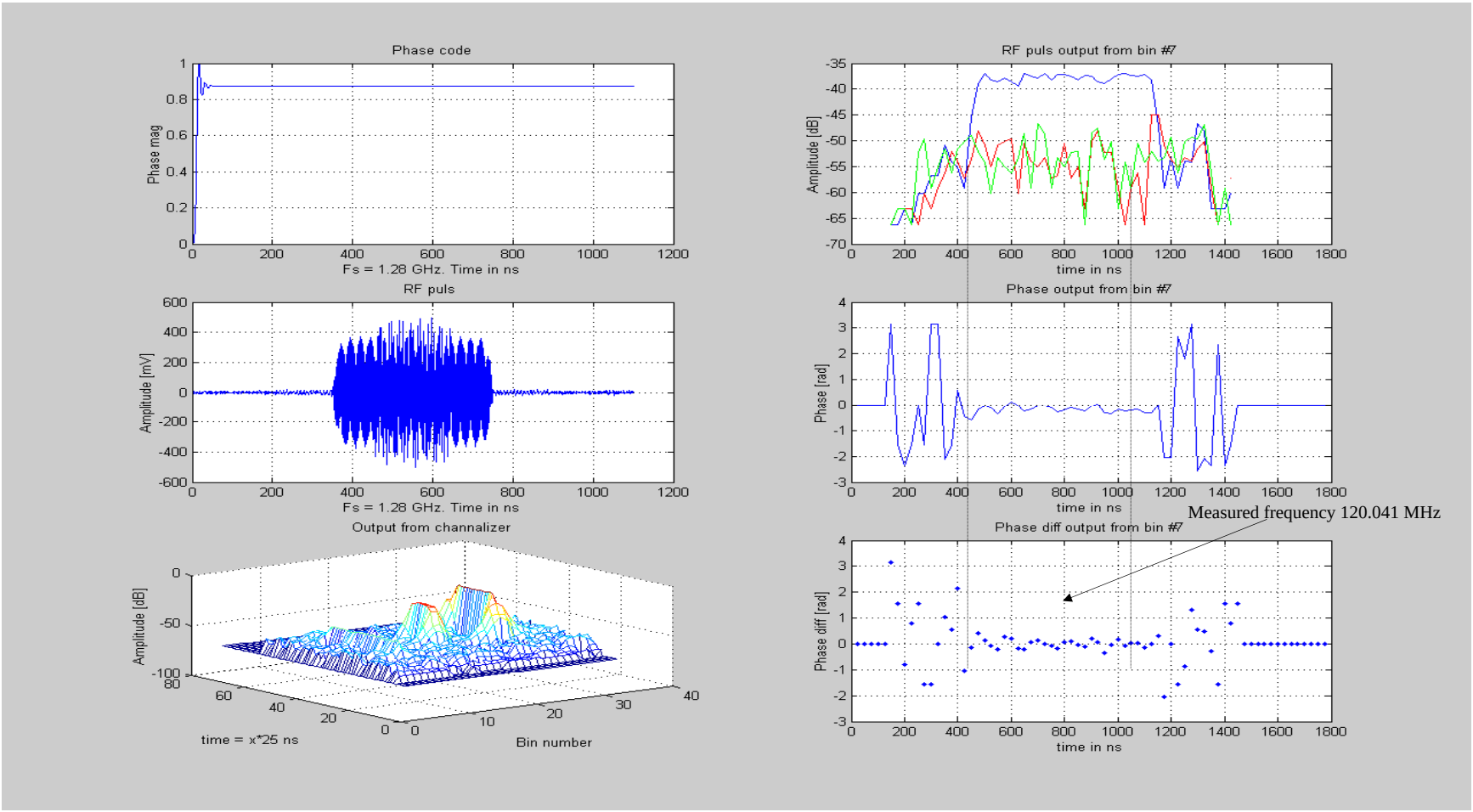
Input shown in the time domain



Channelizer output versus time



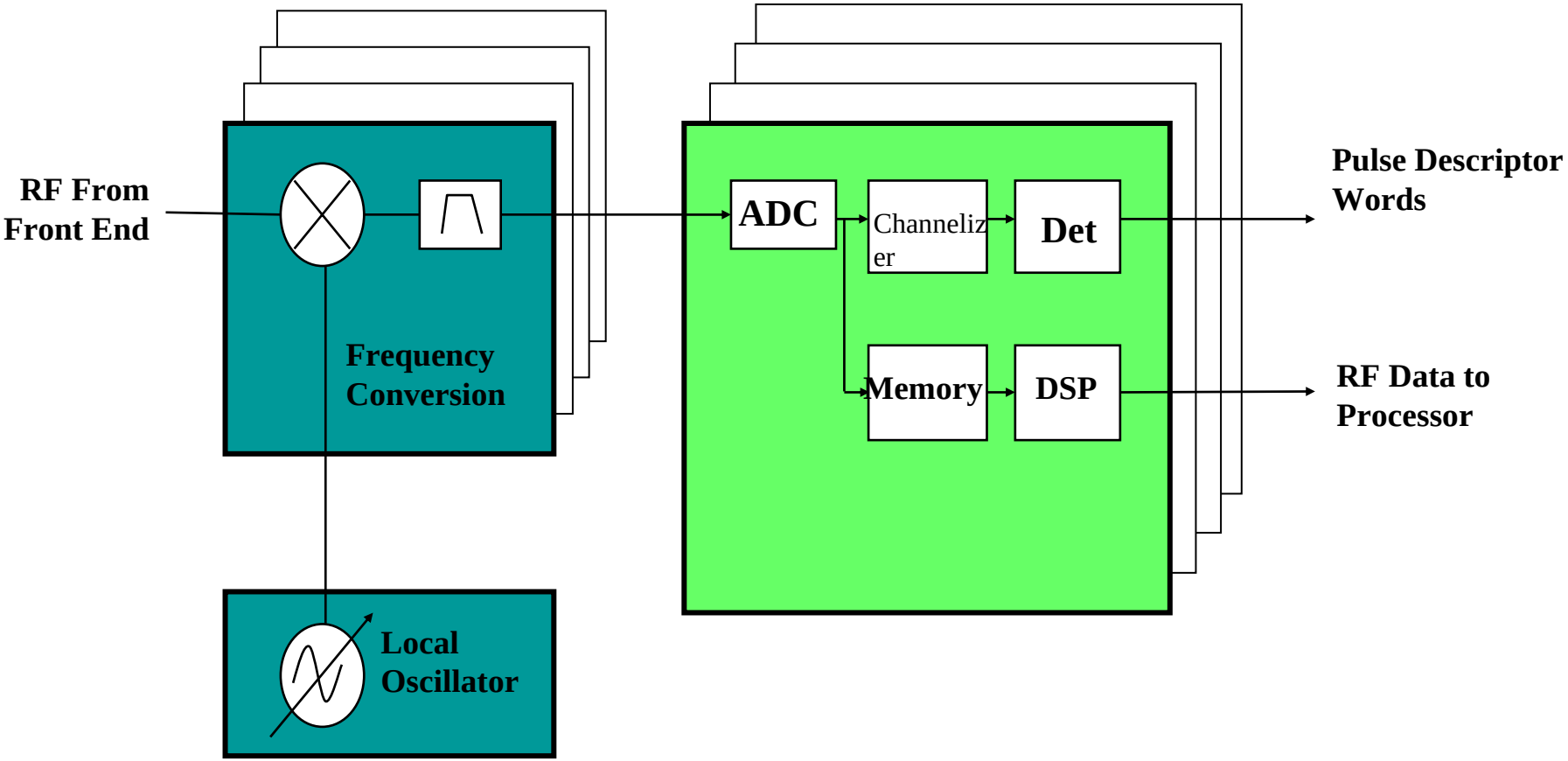
Amplitude and phase vs time of lower amplitude pulse



Summary

- Using multi-bit quantizing of RF signals allows the realization of a channelized receiver with dynamic range up to 50 dB using available multi-bit analog to digital converters.
- Bandwidth of 500 MHz to 1 GHz can easily be realized. Channelizers with 10 to 50 MHz filters are suitable for ESM applications.
- Bandwidth is restricted by technology. This implies the implementation of frequency conversion prior to quantization for radar or EW applications

Example: Digital receiver with 4 RF inputs



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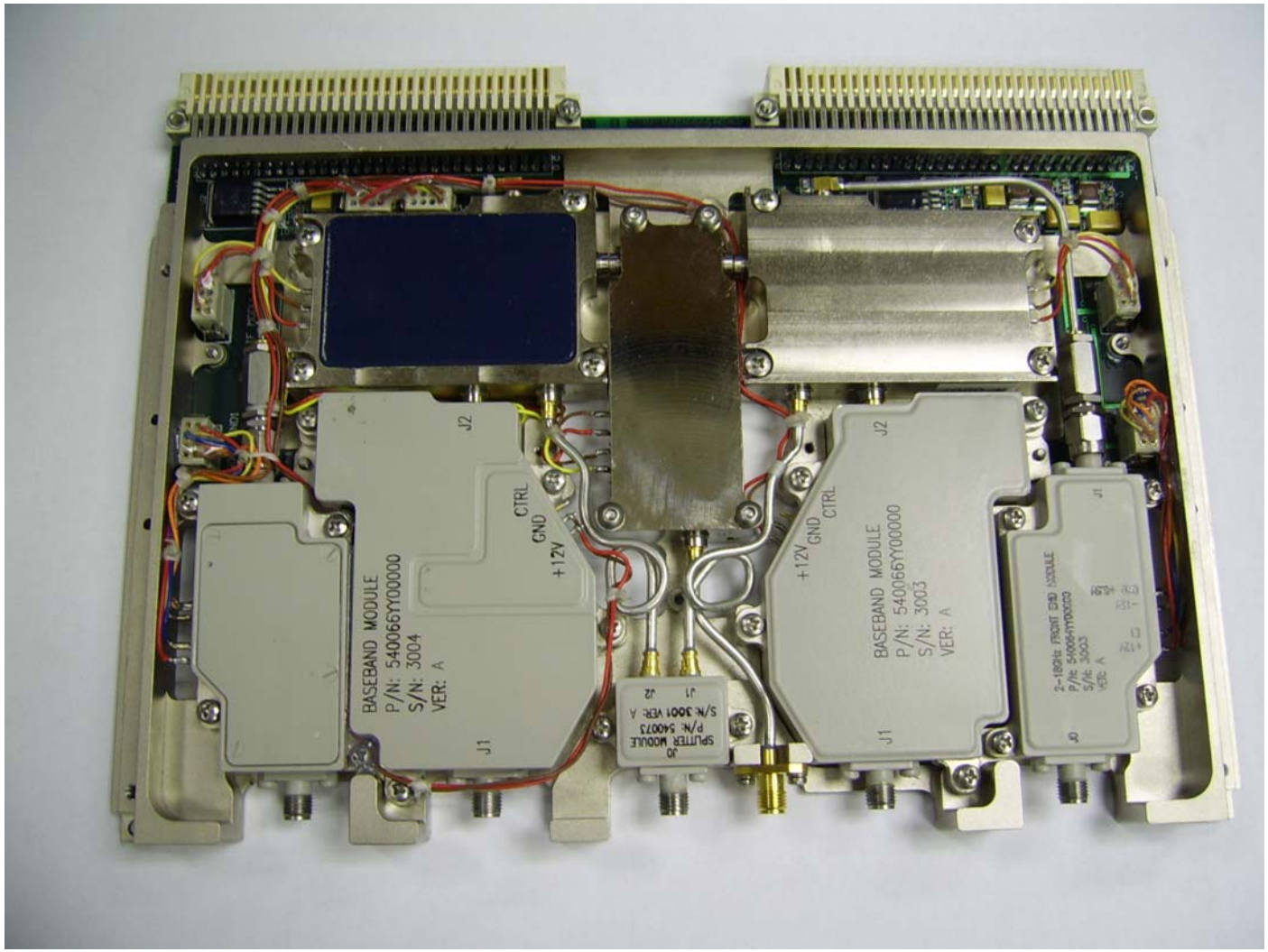
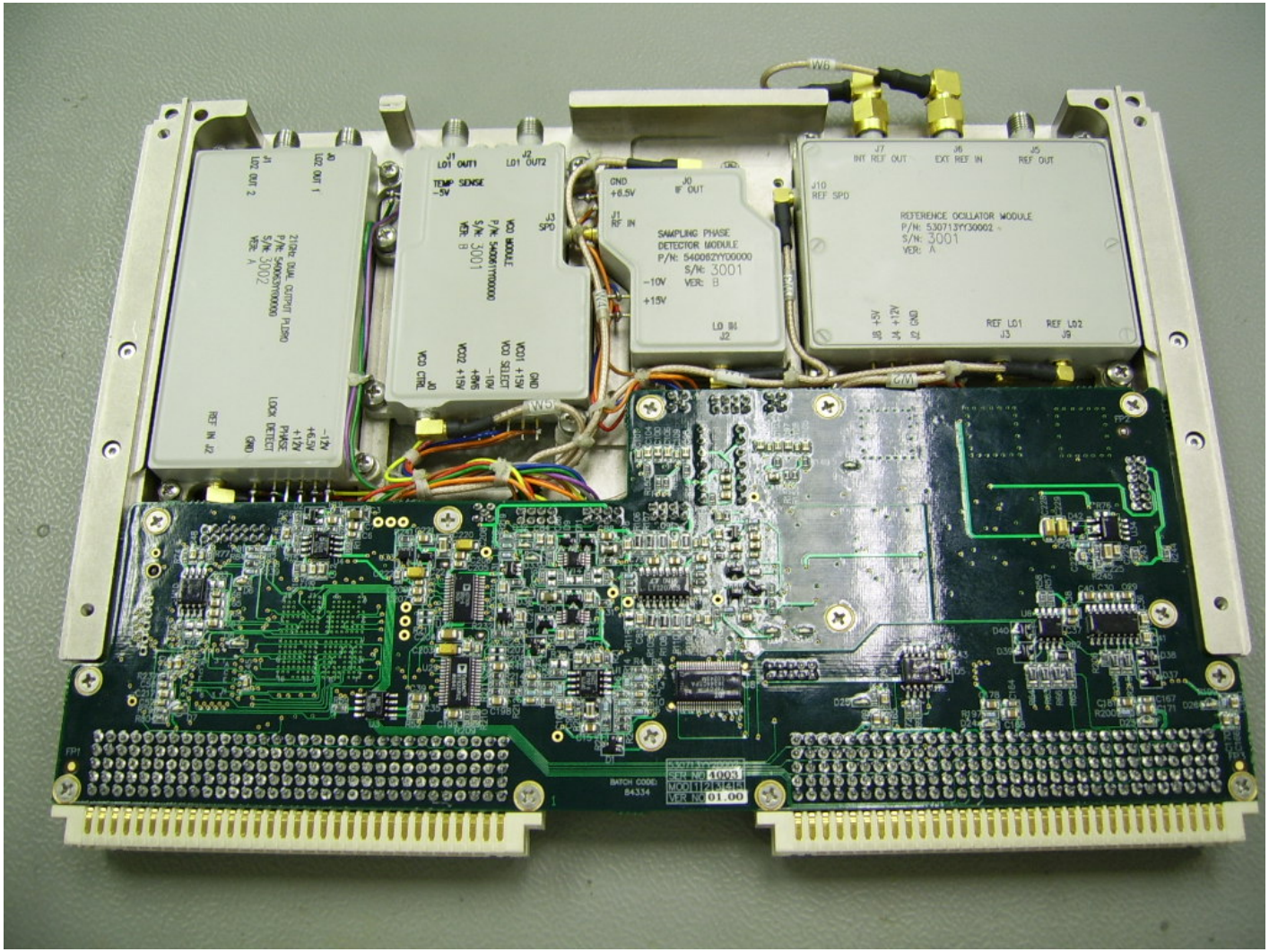
Practical Implementation

- RF circuits for signal conversion to baseband.
  - get cost down
  - get volume/mass down
  - find a synthesizer vendor that is willing to adapt his product to your needs

Two channel converter unit



Synthesized local oscillators



Practical Implementation

- Digital sampling and processing
  - Digital circuits only consume power when they switch between 1 and 0. The faster you switch, the more power is dissipated.
  - All input channels must be processed together for DF algorithms etc. This leads to high density packaging.
  - Get enough logic elements and IO on the board to enable all the calculations required.

Example

- 10 bit ADC (commercially available).
- Sampling rate of 1024 MHz using 10 bits.
- Slowing data by a factor 4.
- Bus width is then 4x10=40 bits, or 80 bits for two channels, or 160 pins if differential signals are used.
- Transport data into the FPGA at 1024/4=256 MHz.
- Channelizer outputs on (say) 25 channels each 12 bits of I and Q data plus strobe implies 1250 pins on FPGA.
- The FFT requires tens of thousands of complex floating point operations for each FFT, to be repeated at a rate of tens of MHz for real time processing
- You are soon running out of logic cells, multiplier cells and pins on the FPGA, long before the max sampling rate of the ADC of more than 2000 MHz is reached.

Example of 4 channel Processor Board

Processor Board Statistics

- PCB
  - 14 layers
  - ~8.500 connections
  - ~7.800 vias
  - ~77m total trace length
- Components
  - ~1.900 components and of which ~1.200 are decoupling capacitors
  - ~11.400 pins (1.517 pins on a single fine pitch BGA)
  - ~400.000 logic cells in 3 FPGA’s
- Sampling clock
  - >1000 MHz, with buses operating at 320, 160 and 40 MHz
- Power consumption
  - ~90W at full operation and worst case temperature

SUMMARY

- The speed of the Analog to Digital converter is generally seen as the limitation to bandwidth.
- This is not the case. In a multibit (8 to 10 bit quantizing) system, the envelope is pushed on many fronts.

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Pushing the bandwidth: Lowering the dynamic range

- In our previous example the 10 bit data was sampled at 1024 MHz and slowed down by a factor 4 to yield a 40 bit bus at a speed of 256 MHz.
- If the bus width and speed is the limitation (of the FPGA), a single bit ADC can be used at 10,24 GHz sampling speed, and slowed down by a factor 40 yielding the same bus speed of 256 MHz.
- This will yield a receiver with no dynamic range, but in which the frequency and phase of the signal can still be measured very accurately for eg. DF purposes. The bandwidth will however be 10 times wider.

Pushing the bandwidth: Simplifying the FFT

- When performing the FFT, thousands of complex floating point operations are required. These take space in the FPGA, and limits the execution speed.

Discrete Fourier Transform (1/2)

Fourier transform:

Transforms function of time to function of frequency

$$Y(f) \equiv \int_{-\infty}^{\infty} y(t) \cdot e^{-j2\pi ft}\, dt$$

Discretization:

$$t(n) = nT_s$$

$$f(k) = k\Delta f = \frac{k}{NT_s}$$

Discrete Fourier Transform (2/2)

Discrete Fourier Transform:
Transforms N sampled points
to N frequency bins

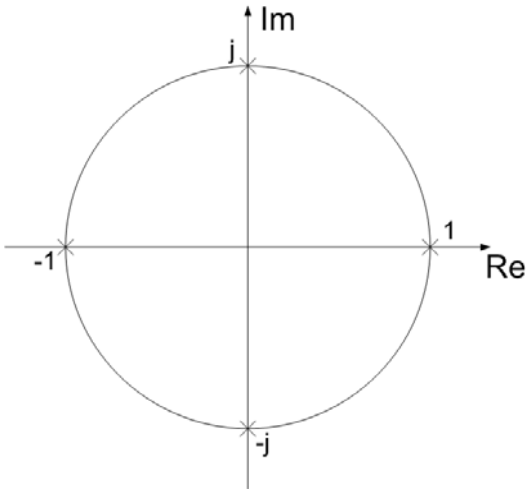
$$Y(k) \equiv \sum_{n=0}^{N-1} y(n) \cdot e^{\frac{-j2\pi kn}{N}} = \sum_{n=0}^{N-1} y(n) \cdot W_N^{kn}$$

$$W_N^{nk} = e^{\frac{-j2\pi nk}{N}} \qquad \begin{cases} n = 0,1,\ldots N-1 \\ k = 0,1,\ldots N-1 \end{cases}$$

- DFT requires ~N^2 complex multiplications
- for N = 128 => ~128^2 > 16000 complex multiplications

Simplified DFT (1/2)

- The Fourier transform involves multiplications between y(n) and W_N^{nk}

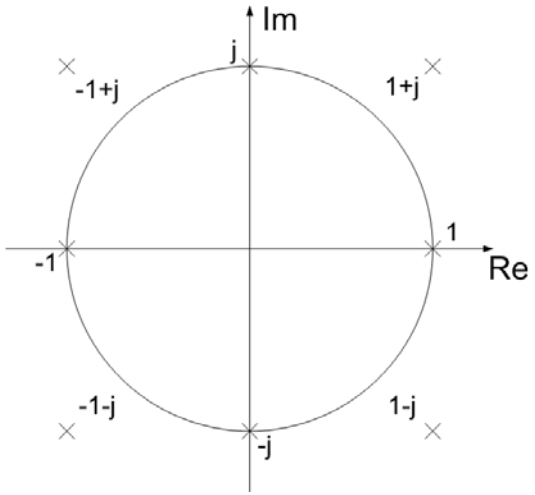


Replace W_N^{nk} with trivial complex numbers:+1, -1, +j, -j

These are easy to multiply with

Simplified DFT (2/2)

- 8-point signal approximation



Real and imaginary part computed separately,
i.e. there are only trivial multiplications

Pushing the bandwidth

- When a simplified FFT is used, nothing is gained by quantizing to more than about 3 bits.
- This could yield a very wideband receiver, with limited dynamic range.
- Much is published about this technique, and techniques to detect and measure simultaneous signals despite the low dynamic range.
- Frequency and phase of the signal is available for DF purposes

CONCLUSION

- Digital receivers is reality, as long as you make use of three very important tools.
  - Know how to read
  - Know how to write
  - Know someone who knows mathematics